IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1. (Currently Amended) A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

a first isolation formed in the bulk device region so as to separate the bulk device;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; ~~and~~

a second isolation in the SOI device region so as to separate the SOI device; and

a boundary layer located at ~~the~~ a boundary between the bulk device region and the SOI device region.

Claim 2. (Original) The semiconductor chip according to claim 1, wherein the bulk growth layer is a silicon bulk growth layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

Claim 3. (Currently Amended) The semiconductor chip according to claim 1, wherein ~~the bulk device region includes a first isolation separating the bulk device, and the SOI device region includes a second isolation separating the SOI device,~~ the first and second isolations ~~being~~ are of substantially the same depth.

Claim 4. (Original) The semiconductor chip according to claim 3, wherein the first and second isolations have a depth reaching the buried insulator.

Claim 5. (Currently Amended) ~~The semiconductor chip according to claim 4, wherein the bulk device region has~~ A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

a pn junction formed in the bulk device region and positioned above ~~the~~ an interface between the base substrate and the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surfaces being positioned at a substantially uniform level; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 6. (Currently Amended) The semiconductor chip according to claim 1, further comprising ~~a first isolation in the bulk device region, a second isolation in the SOI device region, and~~ a third isolation positioned at the boundary and functioning as the boundary layer, wherein the first, second, and third isolations ~~being~~ are of substantially the same depth.

Claim 7. (Currently Amended) ~~The semiconductor chip according to claim 6, wherein~~ A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and

a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as a boundary layer located at a boundary between the bulk device region and the SOI device region, the first, second, and third ~~insulators~~ isolations ~~are~~ being deeper than the buried insulator.

Claim 8. (Currently Amended) The semiconductor chip according to claim 7, wherein the third ~~insulator~~ isolation has a sidewall that is in contact with the buried insulator.

Claim 9. (Currently Amended) ~~The semiconductor chip according to claim 7, wherein the bulk device region has~~ A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

a pn junction formed in the bulk device region and positioned below ~~the~~ an interface between the base substrate and the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surfaces being positioned at a substantially uniform level; ; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 10. (Currently Amended) The semiconductor chip according to claim 1, further comprising ~~a first isolation in the bulk device region, a second isolation in the SOI device region, and~~ a third isolation positioned at the boundary and functioning as the boundary layer, wherein the second isolation ~~being~~ is shallower than the third isolation.

Claim 11. (Currently Amended) The semiconductor chip according to claim 1, ~~further~~ comprising ~~a~~ the first isolation in the bulk device region, and ~~a~~ the second isolation that is shallower than the first isolation, wherein the boundary layer is whichever the first or the second isolation that is positioned closest to the boundary.

Claim 12. (Currently Amended) The semiconductor chip according to claim 11, wherein the second isolation functions as the boundary layer, and has a bottom face that is in contact with the buried ~~oxide~~ insulator.

Claim 13. (Original) The semiconductor chip according to claim 1, further comprising a dummy pattern in the bulk device region near the boundary.

Claim 14. (Currently Amended) ~~The semiconductor chip according to claim 13, wherein the bulk device positioned in the bulk device region includes~~ A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device including a DRAM cell having a trench capacitor, ~~and~~ is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surfaces being positioned at a substantially uniform level;

a boundary layer located at a boundary between the bulk device region and the SOI device region; and

a dummy pattern formed in the bulk device region near the boundary, the dummy pattern ~~is~~ being a dummy capacitor.

Claim 15. (Original) The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part.

Claims 16-28 (Withdrawn)

Claim 29. (New) The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor and a MOSFET, wherein the MOSFET is positioned between the DRAM cell and the boundary layer.

Claim 30. (New) The semiconductor chip according to claim 1, wherein the bulk growth layer is a silicon germanium bulk growth layer.

Claim 31. (New) The semiconductor chip according to claim 1, wherein the bulk growth layer includes a silicon bulk growth layer and a silicon germanium bulk growth layer.